

PTO-1449 REPRODUCED INFORMATION DISCLOSURE CITATION IN AN APPLICATION July 15, 2003 (Use several sheets if necessary)	ATTORNEY DOCKET NO. 0717.1063-007	CONTINUATION OF APPLICATION No. 09/465,140	
	APPLICANT Duy-Phach Vu, et al.		
	FILING DATE	CONFIRMATION NO.	GROUP

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)		
AR	Akiyama, M., <i>et al.</i> , "Growth of GaAs on Si and Its Application to Fets and LEDs.", <u>Nat. Res. Soc. Symp. Proc.</u> , 67:53-64 (1986).	
AS	Allen, <i>et al.</i> , "Characterization of Isolated Silicon Epitaxy Material", <u>SPIE</u> , Vol. 945 - Advanced Processing of Semiconductor Devices II (3/17-3/18, 1988).	
AT	Conference Record of the 1991 International Display Research Conference, October 15-17, 1991, <u>IEEE</u> .	
AU	Fan, <i>et al.</i> , "Lateral Epitaxy by Seeded Solidification for Growth of Crystal Si Films on Insulators", <u>Appl. Phys. Lett.</u> , 38, 365, 3-1-81.	
AV	McClelland, <i>et al.</i> , "A Technique for Producing Epitaxial Films on Reusable Substrates", <u>Appl. Phys. Lett.</u> , 37, 560, 9-15-80.	
AW	McDaniel, D.L., <i>et al.</i> , "Vertical Cavity Surface-Emitting Semi-Conductor Laser with CW Injection Laser Pumping", <u>IEEE Photon Technol. Lett.</u> , March 23, 1990.	
AX	Milnes, A.G., "Semiconductor Heterojunction Topics: Introduction and Overview", <u>Solid State Electronics</u> , Vol. 29, 2:99-121 (1986).	
AY	Turner, G., <i>et al.</i> , "High-Speed Photoconductive Detectors Fabricated in Heteroepitaxial GaAs Layers", <u>Mat. Res. Soc. Symp. Proc.</u> , 67:181-188 (1986).	
AZ	Weber, J.P., <i>et al.</i> , "Effects of Layer Thickness Variations on Vertical Cavity Surface-Emitting DBR Semiconductor Lasers", <u>IEEE Photon Tech. Ltr.</u> , March 23, 1990.	
AR2	Yablonovitch, <i>et al.</i> , "Extreme Selectivity in the Lift-Off of Epitaxial GaAs Films", <u>Appl. Phys. Lett.</u> , 51, 2222 12-28-87.	
AS2	Sumiyoshi, <i>et al.</i> , Device Layer Transferred Poly Si TFT Array for High Resolution Liquid Crystal Projector", <u>IEEE</u> , 7.3.1-7.3.4, 1989.	
AT2	Y. Hayashi, <i>et al.</i> , "A New Three Dimensional IC Fabrication Technology, Stacking This Film Dual-CMOS Layers", <u>IEEE IDEM</u> , pps. 657-660, 1991.	
AU2	"3-D Chip on Chip Stacking", <u>Semiconductor International</u> , December 1991.	

EXAMINER 3/3/03	DATE CONSIDERED 3/3/03
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